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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/745,480	12/26/2000	Yukiyoshi Hikichi	862.C2078	1850

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EXAMINER	
GRANT II, JEROME	
ART UNIT	**PAPER NUMBER**
2626	

DATE MAILED: 09/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/745,480	HIKICHI, YUKIYOSHI	
	Examiner	Art Unit	
	Jerome Grant II	2626	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4, 8-20, 24-32* is/are rejected.

7)☒ Claim(s) *5-7 and 21-23* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

JEROME GRANT
PRIMARY EXAMIN

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *09-16-04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

1. With respect to claim 1, Hayashi teaches an image processing apparatus 1500, comprising: a data input means 1512/1501 for inputting and storing image data in memory 1513; addition means 1503 as claimed; and control means 1511 for controlling access to the memory and said addition means 1503, wherein said control means 1511 controls said data input means and said addition means so as to substantially simultaneously execute the input means and the addition means. This feature is inherent by circuit design and clock speed of the controller. Furthermore, circuit 2200 shows the controller for synthesizing input and added code data according to paragraph 235. Circuit 2200 is the decoder and circuit 1500 (figure 15) is the encoder. Both employ substantially simultaneous processing of the input and addition means as taught and suggested by figures 15 and 22.

With respect to claims 2 and 18, See the encoder 1500 shown by figure 15. Furthermore, circuit 2200 shows the controller for synthesizing input and added code data according to paragraph 235. Circuit 2200 is the decoder and circuit 1500 (figure 15) is the encoder. Both employ substantially simultaneous processing of the input and addition means as taught and suggested by figures 15 and 22.

With respect to claims 3 and 19, Hayashi teaches when said data input means 1512/1501 and said addition means 1503 simultaneously access the memory 1513,

said control means 1511 controls the access by performing bus arbitration (switching signals) to and from the input means and store means (also limitations which are inherent by figure 15).

With respect to claims 4 and 20, Hayashi teaches when said data input means 1512/1501 and said addition means 1503 simultaneously access the memory 1513, said control means 1511 controls the access by performing bus arbitration (switching signals) to and from the input means and store means (also limitations which are inherent by figure 15). Furthermore, time division multiplexing is an inherent feature of the control means since the controller must control a plurality of operating elements in a system at substantially the same time. A single clock speed is high enough to exchange with plural processes over the same time.

With respect to claims 8 and 24, Hayashi teaches the predetermined code as claimed, see the digital watermark which identifies the machine that made the copy at paragraph 231.

With regard to claims 10 and 26, see paragraph 156.

With respect to claims 11 and 27, Hayashi teaches image formation means 1505 for forming an image on the basis of the image data which is stored in said memory

1513 and to which the predetermined code is added, wherein the control means 1511 controls access to the memory and image forming means.

With respect to claims 12 and 28, Hayashi teaches an image input means 1512/1501; a memory 1513; an image processing means 1503 for adding a predetermined code to the image data held in memory; and control means 1511 for controlling access to the memory and said addition means 1503, wherein said control means 1511 controls said data input means and said addition means so as to substantially simultaneously execute the input means and the addition means. This feature is inherent by circuit design and clock speed of the controller. Furthermore, circuit 2200 shows the controller for synthesizing input and added code data according to paragraph 235. Circuit 2200 is the decoder and circuit 1500 (figure 15) is the encoder. Both employ substantially simultaneous processing of the input and addition means as taught and suggested by figures 15 and 22.

With respect to claims 13 and 29, Hayashi teaches an image formation device 1505 for forming an image o the basis of the image data which is held in said memory device 1513 and to which the predetermined code is added, wherein said control device 1511 controls access to the memory device by said image formation device, see figure 15.

With respect to claims 14 and 30, Hayashi teaches input means 1512/1501 for inputting image data, addition means 1503 for adding a predetermined code to image

data, a memory 1513 for holding image data and control means 1511 for controlling access to the plurality of components in the input means 1512/1501 and addition means 1503 comprising: the data input step of storing (via memory 1513) the image data input by the data input mans in the memory; and the addition step of causing the addition means to add the predetermined code (watermark) to the image data stored in the memory. Hayashi teaches Circuit 2200 is the decoder and circuit 1500 (figure 15) is the encoder. Both employ substantially simultaneous processing of the input and addition means as taught and suggested by figures 15 and 22.

With respect to claims 15 and 31, Hayashi teaches a control program ROM or memory in OS, see paragraphs 267 and 268, in an image processing apparatus having input means for inputting image 1512/1501, addition means 1503 for adding a predetermined code to the image data, a memory 1513 for holding the image data, and control means for controlling access to the memory by a plurality of components including the data input means and the addition means, comprising: a code (para. 266) for inputting a storage step in the memory, see elements 1512/1501 and 1503; and a code (see para. 266) of the addition step of causing the addition means to add the predetermined code, wherein circuit 2200 is the decoder and circuit 1500 (figure 15) is the encoder. Both employ substantially simultaneous processing of the input and addition means as taught and suggested by figures 15 and 22.

With respect to claims 16 and 32, the storage medium is a ROM, see paragraphs 267 and 268.

With respect to claim 17, Hayashi teaches an image processing apparatus 1500 comprising: data input means 1512/1501 for inputting image data and storing the image data in a memory; addition means 1503 for adding a predetermined code to the image data stored in the memory (watermark).; and control means 1511 for controlling access to the memory by said input and addition means, wherein circuit 2200 is the decoder and circuit 1500 (figure 15) is the encoder. Both employ substantially simultaneous processing of the input and addition means as taught and suggested by figures 15 and 22.

2.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 9 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hayashi.

Hayashi teaches all of the subject matter upon which the claim depends except for the specific use of a code being yellow.

Hayashi does provide generation of a specific code via a watermark code according to paragraph 231. Even though Hayashi does not teach the specific watermark code as yellow, the use of yellow watermarks or infrared inks that are difficult to detect by the human eye, would have been recognized as art equivalent means of generating a watermark. Thus, it would have been obvious to replace the water mark code specifically explained by Hayashi with a yellow watermark for the purpose of generating the predetermined code.

3.

Claims Objected as Containing Allowable Matter

Claims 5-7 and 21-23 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

4.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jerome Grant II whose telephone number is 703-305-4391. The examiner can normally be reached on Mon.-Fri. from 9:00 to 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kimberly A Williams, can be reached on 703-305-4863. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JEROME GRANT II
PRIMARY EXAMINER
J. Grant II